AMENDMENTS TO THE DRAWING

A Replacement formal drawing of Figure 14 is submitted concurrently herewith under a separate cover letter.

REMARKS

In view of the above amendments and the following remarks, reconsideration of the objection and rejection and further examination are respectfully requested.

The specification and abstract have been reviewed and revised to improve their English grammar. The amendments to the specification and abstract have been incorporated into a substitute specification and abstract. Attached are two versions of the substitute specification, a marked-up version showing the revisions, as well as a clean version. No new matter has been added.

Proposed drawing amendments are submitted herewith under a separate cover letter. Specifically, Figure 14 has been amended to correct various spelling errors. These drawing amendments are editorial in nature and do not add new matter to the application.

Original claims 1-7 have been cancelled without prejudice or disclaimer to the subject matter contained therein and replaced by new Claims 8-11.

Original claim 5 was objected to as containing informalities. Since claim 5 has been cancelled it is respectfully submitted that this objection is no longer applicable.

Claims 1-7 were rejected under 35 U.S.C. § 102(b) as being anticipated by Inoue et al. (U.S. 2002/0113885 A1). This rejection regarding claims 1-7 is considered moot based on their above-mentioned cancellation. Further, this rejection is clearly inapplicable to new claims 8-11 for the following reasons.

New independent claim 8 recites an image processing apparatus including, in part, (1) an image storage unit operable to store an image as a plurality of lines, each line having a plurality of pieces of pixel data sequentially arranged, (2) a first reading out unit operable to sequentially read out, from the image storage unit, the plurality of pieces of pixel data of each line and operable to sequentially output the plurality of pieces of pixel data sequentially read out, (3) a second reading out unit operable to read out one or more pieces of pixel data located at a head of each line of the plurality of the lines and operable to output the one or more pieces of pixel data read out, and (4) an arithmetic unit operable to execute an arithmetic process for generating output pixel data using the pixel data output from the first reading out unit and the second reading out unit. It is noted that, according to claim 29, before the arithmetic unit completes the arithmetic process for generating a last output pixel data for one of the plurality of lines using the pixel data

output from the first reading out unit, the second reading out unit is operable to read out the one or more pieces of the pixel data located at the head of a next line, and it is noted that the arithmetic unit is operable to use the pixel data output from the second reading out unit when executing the arithmetic process for generating a first output pixel data for the next line. The Inoue reference fails to disclose or suggest the first and second reading out units and the arithmetic unit as recited in independent claim 8.

The Inoue reference teaches an image processing device which includes an image splitting processing circuit for performing image splitting on an image (i.e., creating sub-images), an image processing circuit for performing parallel image processing of each of the split images (i.e., sub-images), and an image compression circuit for compressing in parallel each of the sub-images that are output from the image processing circuit (see abstract). Specifically, Inoue teaches that the image splitting circuit 15 (including image splitting circuits 15a-15h) splits an image signal into eight image regions and teaches that image processing circuits 16a-16h perform parallel processing to produce output signals for each of the eight image regions (see paragraph [0074], lines 8-14, and Fig. 1).

Specifically, Inoue teaches that each image splitting circuit 15a-15h includes FIFO memories 22 wherein respective signals are simultaneously input into the FIFO memories 22 of each image splitting circuit 15a-15h from an image conversion circuit 14, and then respective split image signals are sent from each respective FIFO memory 22 to each respective image processing circuit 16a-16h (see paragraph [0091]-[0094], and Fig. 5). Based on this configuration, the image processing device of Inoue teaches that a main image is split into sub-images by feeding signals representing each of the sub-images is into respective FIFO memories of respective image splitting devices and then respective image data is sent from each FIFO memory to a respective image processor for parallel processing of the image data of each of the sub-images.

Regarding the management of image data, although Inoue teaches splitting a main image into sub-images and simultaneously reading out information from each of the sub-images into a separate FIFO memory to be processed by separate respective image processors, Inoue does not disclose or suggest reading out pieces of pixel data of each line of a single image and subsequently processing the pixel data using the first and second reading out units and the arithmetic unit, as recited in claim 8.

Regarding the processing of image data, although Inoue teaches that data from each sub-image is simultaneously read into each FIFO memory and then sent to respective image processors for parallel processing of the data from the multiple sub-images, Inoue does not disclose or suggest an image processing apparatus which includes a first reading out unit that sequentially reads out a plurality of pieces of pixel data of each line, wherein, before the arithmetic process of the arithmetic unit generates the last output of pixel data for one line using the pixel data output from the first reading out unit, the second reading out unit reads out one or more pieces of pixel data from the head of the next line. In other words, reading data from multiple sub-images into respective FIFO memories and then from the respective FIFO memories to respective (separate) image processors does not disclose or suggest that the second reading out unit reads out one or more pieces of pixel data located at the head of the next line before the arithmetic unit generates the last output pixel data of a prior line using pixel data output from the first reading unit. Thus, in the context of processing data from a specific portion of an image, it is clear that Inoue does not disclose or suggest the above described features of claim 8.

It is noted that the image processing apparatus of claim 29 results in an increased efficiency when processing image data by reducing a delay when transitioning from a (present) line to a next line. This increased efficiency is evident because, prior to the arithmetic unit completing image processing for a last pixel of a (present) line, a second reading out unit reads out pieces of pixel data from a next line. In contrast, the Inoue reference does not disclose an invention which results in an increased efficiency when processing image data, as discussed above, because the image data is not read from a next line of pixel data prior to a completion of processing a present line of pixel data.

In view of the above, it is respectfully submitted that the Inoue reference does not anticipate the invention as recited in new claim 8. Furthermore, Inoue does not suggest the above limitations of independent claim 8. Therefore, it would not have been obvious to one of ordinary skill in the art to modify the Inoue reference so as to obtain the invention of new independent claim 8. Accordingly, it is respectfully submitted that new independent claim 8 and the claim that depends therefrom are clearly allowable over Inoue.

New independent claim 10 is a method version of new independent apparatus claim 8. Thus, for reasons similar to those discussed above, it is respectfully submitted that independent claim 10 and the claim that depends therefrom are allowable over the Inoue reference.

In view of the above amendments and remarks, it is submitted that the present application is now in condition for allowance and an early notification thereof is earnestly requested. The Examiner is invited to contact the undersigned by telephone to resolve any remaining issues.

Respectfully submitted,

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